Cycle-Free FPGA Routing Graphs

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Accurate timing characterization of FPGA routing resources, i.e. wires and switches, is critical to achieving high quality of results from FPGA routing tools. Although the composition and connectivity of the routing resources are easily extracted from an FPGA's architecture, post-layout timing characterization of the FPGA's wires and switches (NOT the design being mapped onto the FPGA) with EDA tools is a challenging task due to the large quantity of combinational loops (cycles in the routing graph). Likewise, the use of EDA tools is severely limited when constructing new FPGA architectures.

This work addresses the challenge by proposing an algorithm to construct cycle-free FPGA routing graphs. A cycle-free FPGA routing graph is achieved by logically ordering wires and intelligently removing or rearranging a small fraction of the switch block connections in order to break cycles. The proposed approach enables constraining the timing of all routing resources, which is otherwise impossible due to the combinational loops. This technique can be applied to post-layout static timing analysis (STA) of existing FPGAs, significantly reducing the complexity and improving the accuracy of the analysis. In addition, this cycle-free approach can be adopted when designing new FPGAs, transforming costly hand layout into an automated step compatible with commercial ASIC EDA tools.

Keywords: FPGA; FPGA Routing Graph; FPGA Timing Characterization

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